

IN THE CLAIMS:

Following is a complete listing of all claims in the application, with an indication of the status of each:

1 Claim 1 (Currently Amended). A vertical field effect transistor including
2 a semiconductor pillar conduction channel,
3 gate electrodes in trenches adjacent said semiconductor pillar,
4 a layer of insulator adjacent said gate electrodes and opposite said semiconductor
5 pillar,
6 sidewalls adjacent said semiconductor pillar above said gate electrodes in said

7 trenches,
8 insulator material in said trenches above said gate electrodes and **adjacent**
9 **between** said sidewalls **and said layer of insulator**, said insulator material being
10 selectively etchable relative to said sidewalls and said semiconductor pillar.

1 Claim 2 (Currently Amended). A vertical transistor as recited in claim 1, further
2 including isolation material adjacent said layer of insulator **and** surrounding said vertical
3 transistor, said isolation material being selectively etchable relative to said layer of
4 insulator.

1 Claim 3 (Currently Amended). A vertical transistor as recited in claim 2, further
2 including
3 a contact formed in an opening in said isolation material adjacent said **layer of**
4 insulator to a conductive region at an end of said pillar.

1 Claim 4 (Original). A vertical transistor as recited in claim 1, further including
2 a contact formed in an opening to an end of said pillar, and
3 a contact formed in an opening adjacent to and extending above said pillar to said
4 gate structure and insulated from said pillar by an insulating sidewall on said pillar.

fig. 22C
37C

OK

not ok,
should be
insulator
material
[2020]
fig. 22C

1 Claim 5 (Original). A vertical transistor as recited in claim 1, further including
2 a spacer in said trench between said gate structure and a bottom of said trench.

3 Claim 6 (Previously Presented). An integrated circuit device including
4 isolation material surrounding transistor locations in a substrate,
5 vertical field effect transistors formed at said transistor locations and having a gate
6 electrode structure formed in a trench,
7 a layer of insulator material in said trench between said isolation material and said
8 gate electrode structure, said isolation material being selectively etchable relative to said
9 layer of insulator and
10 a contact opening formed along an interface of said layer of insulator material and
11 said isolation material.

1 Claim 7 (Original). A device as recited in claim 6, wherein said gate structure includes
2 dual gate electrodes extending on opposite sides of a conduction channel.

1 Claim 8. (Currently Amended) A device as recited in claim 6, further including
2 a contact formed in said contact opening in said isolation material adjacent said
3 layer of insulator and extending to a conductive region extending below said pillar.
*Same as
claim 3*

1 Claim 9 (Original). A device as recited in claim 6, further including
2 a contact formed in an opening to an end of said pillar, and
3 a contact formed in an opening adjacent to and extending above said pillar to said
4 gate structure and insulated from said pillar by an insulating sidewall on said pillar.

1 Claim 10 (Currently Amended). A device as recited in claim ~~6~~ 6, further including
2 a spacer in said trench between said gate structure and a bottom of said trench.
DK

1 11 (Withdrawn). A method of making a semiconductor device including a field
2 effect transistor, said method including steps of
3 forming a semiconductor pillar in a trench in a body of a first insulating material,
4 said trench extending to a layer of semiconductor material,
5 forming a layer of a second insulating material on walls of said trench, and
6 etching a contact opening to said semiconductor material through said first
7 insulating material selectively and adjacent to said second insulating material.

1 12 (Withdrawn). A method as recited in claim 11, including further steps of
2 forming a gate structure adjacent sides of said pillar,
3 forming layers and/or sidewalls of selectively etchable materials over said gate
4 structure and said pillar, and
5 forming contact openings to an end of said pillar and said gate structure by
6 selective etching of said layers at locations above and adjacent said pillar, respectively.

1 13 (Withdrawn). A method as recited in claim 11, including further steps of
2 defining a height of said pillar by thickness of a layer of sacrificial material.

1 14 (Withdrawn). A method as recited in claim 13, wherein said sacrificial material is
2 germanium oxide.

1 15 (Withdrawn). A method as recited in claim 11, wherein said step of forming said
2 pillar is performed by epitaxial semiconductor growth in a trench.

1 16 (Withdrawn). A method as recited in claim 11, wherein said step of forming said
2 pillar is performed by etching of a layer of semiconductor material.

1 17 (Withdrawn). A method as recited in claim 11, including a further step of
2 limiting a dimension of said pillar by a distance between isolation structures.

3 Claim 18 (Original). A transistor comprising
4 a substrate,
figs. 36A-5
36C, 6
38A-38C 7 a first diffusion,
 a second diffusion above said first diffusion,
 a channel extending vertically between said first diffusion and said second
8 diffusion,
9 a gate structure extending on at least one side of said channel, and
10 a contact to said first diffusion borderless to said gate structure.

1 Claim 19 (Original). A transistor as recited in claim 18, wherein said transistor is a
2 vertical transistor and wherein said first diffusion is formed in said substrate and said
3 second diffusion is formed on the channel.

1 Claim 20 (Previously Presented). A transistor as recited in claim 18, wherein said gate
2 structure extends on two sides of said channel.

1 Claim 21 (Original). A transistor as recited in claim 19, wherein a contact to said gate
2 extends above and on two sides of said second diffusion.

1 Claim 22 (Original). A transistor as recited in claim 19, further including separate
2 contacts to separate portions of said gate structure on different sides of said channel.

1 Claim 23 (Original). A transistor as recited in claim 18, wherein said gate structure
2 extends on at least three sides of said channel.

1 Claim 24 (Original). A transistor as recited in claim 18, further including a contact to
2 said second diffusion borderless to said gate structure.

1 Claim 25 (Original). A transistor as recited in claim 18, wherein said transistor

2 comprises a pillar of single crystal silicon having an edge.

1 Claim 26 (Original). A transistor as recited in claim 25, wherein said pillar comprises
2 said first diffusion, said channel and said second diffusion, said gate structure extending
3 adjacent said pillar.

1 Claim 27 (Original). A transistor as recited in claim 26, wherein said first diffusion
2 extends into single crystal silicon beneath said pillar and extends below said gate
3 structure for formation of a contact adjacent said gate structure.

1 Claim 28 (Original)... A transistor as recited in claim 26, further comprising
2 an insulator adjacent said gate structure, wherein said contact to said first
3 diffusion comprises a conductive layer adjacent said insulator.

OK 1 Claim 29 (Currently Amended). A transistor as recited in claim 26, wherein a
2 contact to said gate structure is borderless to said second diffusion.

1 Claim 30 (Currently Amended). A transistor as recited in claim 26, wherein said
OK 2 contact to said second diffusion comprises extends adjacent to a spacer which is self-
3 aligned to said edge.

1 Claim 31 (Original) A transistor as recited in claim 26, wherein said pillar extends
2 above said gate structure.

1 Claim 32 (Original). A transistor as recited in claim 18, further comprising
2 an isolation structure, wherein said transistor is self-aligned to said isolation
3 structure.

OK 1 Claim 33 (Currently Amended). A transistor as recited in claim 18, further

2 comprising
3 a contact between said first diffusion and another diffusion forming part of a
4 second transistor, wherein said contact between said first diffusion and said another
5 diffusion extends over an area of insulation between said first transistor and said second
6 transistor.

1 Claim 34 (Original). A transistor as recited in claim 33, wherein said insulation
2 comprises an etched and deposited isolation structure.

1 Claim 35 (Original). A transistor as recited in claim 34 wherein said substrate comprises
2 SOI having buried oxide isolation and wherein said insulation comprises said buried
3 oxide isolation.

1 Claim 36 (Original). A transistor as recited in claim 33, wherein said first transistor and
2 said second transistor comprise an inverter and wherein said contact to said first diffusion
3 is a contact to said inverter.

1 Claim 37 (Original). A transistor as recited in claim 18, wherein said gate structure
2 comprises a continuous interior wall entirely surrounding said channel and spaced
3 therefrom by a dielectric layer.

1 Claim 38 (Original). A transistor as recited in claim 18 wherein said gate structure is
2 self-aligned to said channel.

1 Claim 39 (Original). A transistor as recited in claim 18 wherein said first diffusion
2 comprises a dopant species provided separately from said second diffusion.

1 Claim 40 (Original). A transistor as recited in claim 18, wherein said channel is of sub-
2 lithographic width.

1 Claim 41 (Original). A transistor as recited in claim 18, wherein said first diffusion
2 includes
3 top and side surfaces covered by a dielectric material,
4 a borderless opening at least through a portion of the dielectric material on said
5 top surface, and
6 a first diffusion contact formed in the opening.

1 Claim 42 (Original). A transistor as recited in claim 18, wherein said second diffusion
2 includes
3 top and side surfaces covered by a dielectric material,
4 a borderless opening at least through a portion of the dielectric material on said
5 top surface, and
6 a second diffusion contact formed in the opening.

1 Claim 43 (Original). A transistor as recited in claim 18, wherein said gate structure
2 includes
3 top, bottom and side surfaces covered by a dielectric material,
4 a borderless opening at least through a portion of the dielectric material on said
5 top surface, and
6 a gate contact formed in the opening.

1 Claim 44 (Original). A transistor as recited in claim 18, wherein said first diffusion, said
2 second diffusion and said gate structure each include a borderless contact.